SST-200 GNSS Baseband Correlator

Features

- 16-channel GNSS Baseband Correlator
- Supports GPS, GLONASS and QZSS Baseband correlation
- Delivers extremely fast fix times
- Interfaces with standard GPS and GLONASS RF front-end chips
- Supports external sample clock
- SPI interface for data exchange – can be interfaced to any processor
- 2.5V I/O (3.3V tolerant), 1.2V Core Supply voltage
- 5mm x 5mm TQFN package
- Fully ROHS compliant
- -40 to +85 C operating temperature

SST-200

Product Description

SST-200 is a miniature high performance GPS / GLONASS / QZSS Baseband Correlator aimed at interfacing with any standard GPS or GLONASS RF front-end and a General Purpose Processing element to realize a GPS / GLONASS Receiver.

SST-200 is a 16-channel implementation capable of acquiring and tracking up to 16 GPS or GLONASS or QZSS satellites simultaneously. It receives a 2-bit digitized IF from the RF front-end and delivers the correlation results over the SPI interface.

SST-200 is designed to accept an external clock of 16.368MHz and can generate its internal clocks for processing.

An SPI port on the SST-200 supports glue-less communication interface with any general-purpose processor. Through this interface, it is possible to read the correlation results from and to configure the SST-200. The SPI port supports different clock polarity/phase options and can communicate at a maximum clock speed of 40MHz. A full-duplex SPI port on the processor is recommended for interfacing with the SST-200.

The SST-200 can be configured to function as a GPS or GLONASS or QZSS correlator through a control pin.

SST-200 Hardware Details

A typical block diagram of the SST-200 is shown below.

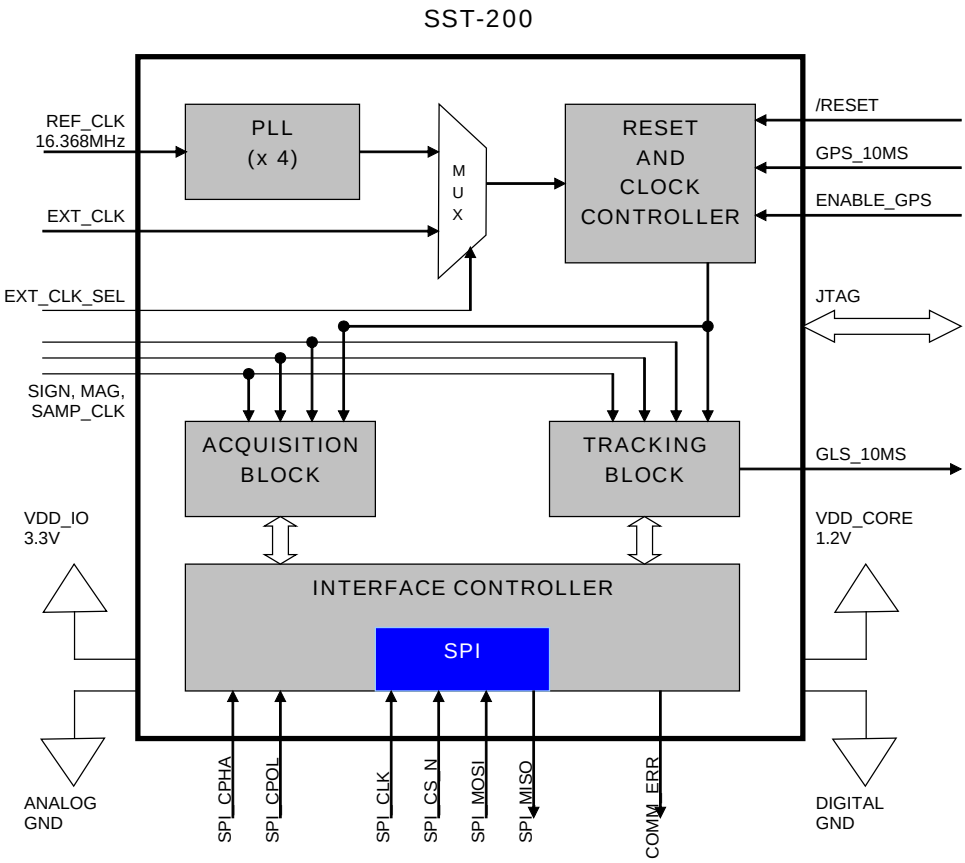

Figure 2. Block Diagram of the SST-200

The SST-200 is built around a few basic blocks and interfaces.

The Reset and Clock Controller block is responsible for handling the Reset input and also defines the operational mode of the chip. The SST-200 can be configured to operate as either a GLONASS correlator or as a GPS / QZSS correlator. This block can also be synchronized to a companion GPS correlator (AST-230) through a GPS_10MS input pin. The clock input to this block is derived from an internal PLL or directly from an external source. The SST-200 works out of a 16.368MHz reference clock input to the PLL or directly from a 65.472MHz external clock.

The interface to the RF front-end is achieved through the SIGN, MAG and SAMP_CLK pins. The digitized IF from the GLONASS or GPS front-end along with the sampling clocks are fed to both Acquisition and Tracking blocks. These blocks are controlled from the Reset and Clock Controller. The Acquisition and Tracking blocks work on 16 independent channels and generate the correlation results.

The SST-200 provides an industry standard SPI interface to exchange the information with a host processor. The SPI port configuration such as clock phase and polarity can be set through dedicated hardware pins. The SPI interface can work upto 40MHz. Any error in communication is flagged off through a pin.

The SST-200 is packaged in a 5mm x 5mm TQFN with 40 functional and power supply pins.

Circuit Interconnection Diagram

The below interface diagram illustrates the realization of a GLONASS receiver using SST-200. The other key components used in the implementation are AST-GLSRF, a GLONASS RF Front-end chip and any general-purpose processor with SPI support.

The diagram illustrates all the terminations required for the various configuration pins in addition to the connectivity to the RF front-end and the host processor.

The power supply inputs are also indicated.

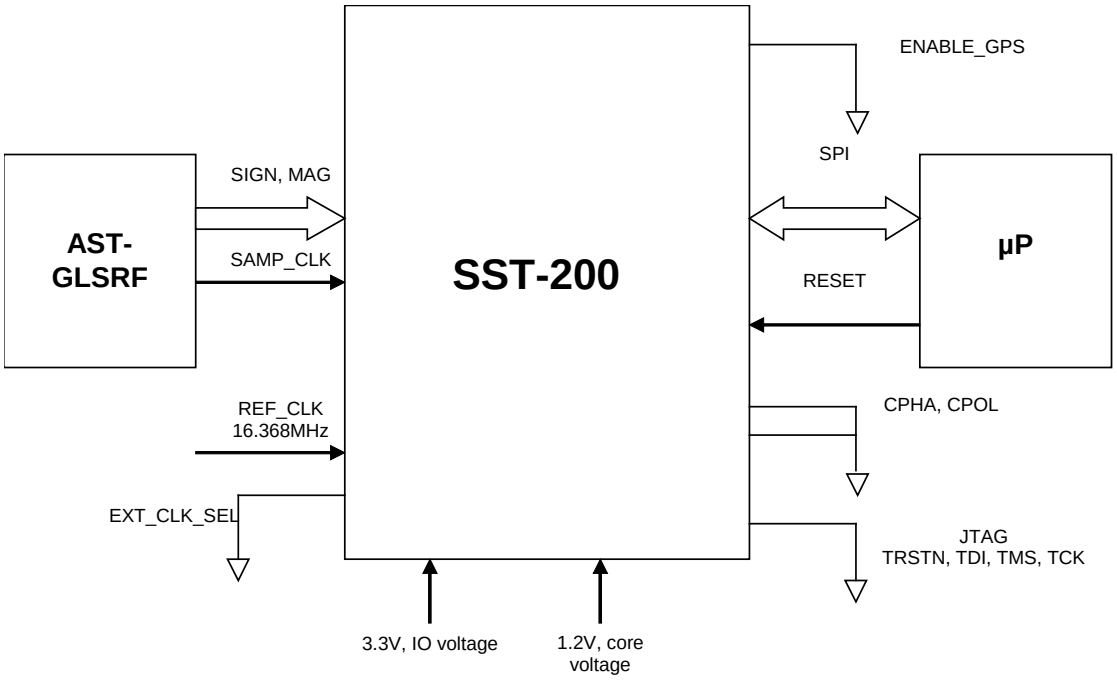

Figure 3. Circuit Interconnection using SST-200

GENERAL	
Acquisition Channels	16
Tracking Channels	16
System Clock Frequency	65.472 MHz
RF INTERFACE	
Interface	2-bit; SIGN, MAG
GLONASS Sampling Clock	26.598MHz
GPS Sampling Clock	16.368MHz
PROCESSOR INTERFACE	
Communication Interface	SPI
Communication Failure Indication	Communication Error Flag
SPI	
Configuration	CS, CLK, MOSI, MISO
Clock	40MHz (Max)
Configuration	Clock Polarity, Clock Phase
Error output	Communication error is transmitted through a dedicated pin
CLOCKS	
System Clock	16.368MHz
Sampling Clock	25.598MHz – GLONASS 16.368MHz – GPS, QZSS
DIGITAL INPUT	
Reset	Active Low Chip Reset
GPS 10ms	Measurement Latch Pulse from the companion GPS correlator
Function Select	Selection between GLONASS or GPS / QZSS functionality
DIGITAL OUTPUT	
GLONASS 10ms	GLONASS Measurement Latch Instant
JTAG	
JTAG	Used only under Test Mode In Functional Mode, TDI, TCK, TMS and TRST lines to be connected to GROUND
POWER SUPPLY	
Core Supply	1.2V
I/O Supply	2.5V (3.3V tolerant)
Electrical	
Supply Current (@ 1.2V)	50mA (peak), 30mA (Tracking)
Ordering Detail	
Ordering Part Number	SST-200

Table 1. Specifications of SST-200

Accord Software & Systems Pvt. Ltd.
37, K.R. Colony, Domlur Layout,
Bangalore - 560 071. INDIA.
Tel: +91 - 80 2535 0105
Fax: +91 - 80 2535 2723
Website: www.accord-soft.com